SESSION 12 – Honolulu Suite
New DRAM Cell Architectures and Design Techniques

Friday, June 18, 10:20 a.m.
Chairpersons: H. Pon, Intel
M. Ikeda, University of Tokyo

12.1 — 10:20 a.m.
SOI Capacitor-Less 1-Transistor DRAM Sensing Scheme with Automatic Reference Generation, M. Blagojevic, M. Pastre, M. Kayal, P. Fazan, S. Okhonin, M. Nagoga and M. Declercq, Swiss Federal Institute of Technology, Lausanne, Switzerland

This paper proposes a sensing scheme with automatic reference generation for SOI capacitorless 1-transistor DRAM. An electrical calibration of the reference current source is implemented using a digital-to-analog converter and a successive approximation algorithm. The automatic reference current generation using the presented scheme makes the sensing of the memory cellstate independent of the BL capacitance mismatch, the memory cell current dispersion and the SA offset.

12.2 — 10:45 a.m.
2T1D Memory Cell with Voltage Gain, W.K. Luk and R.H. Dennard, IBM T.J. Watson Research Center, Yorktown Heights, NY

A 2T1D dynamic memory cell with two transistors (T) and a gated diode (D) is presented. The gated diode acts as a non-linear capacitance which amplifies the internal stored voltage in a read operation, leading to high performance, higher S/N ratio, and low voltage operation. Details about the gated diodestructure, its principle of operations, the memory cell circuits and the array structure are presented, followed by hardware results. (Keywords: Gated diode,CMOS, SOI, 2T1D, memory cell with voltage gain, non-destructive read, gaincell)

12.3 — 11:10 a.m.
A 4.8-ns Random Access 144-Mb Twin-Cell-Memory Fabricated Using 0.11-um Cost-Effective DRAM Technology, H. Noda, S. Miyatake*, T. Sekiguchi**, R. Takemura**, T. Sakata**, K. Saino, Y. Kato, E. Kitamura and K. Kajigaya, Elpida Memory, Inc., Sagamihara, Kanagawa, Japan, *Hitachi ULSI Systems, Tokyo, Japan and **Hitachi, Ltd., Tokyo, Japan

A 144-Mb twin-cell-memory was fabricated using 0.11-um cost-effective DRAM technology. A direct-sense-amp with a three-stage sensing scheme can achieve a random access time of 4.8 ns. The source-separated restore-sense-amp enables a random cycle time of 6.0 ns. The peak bandwidth is 48 Gb/s with separate I/O and simultaneous read/write operations. High performance was also realized using W/WNx dual-gate CMOS technology with a p+ gate memory-cell-transistor.

12.4 — 11:35 a.m.
A 130nm 1.1V 143MHz SRAM-like Embedded DRAM COMPILER with Dual Asymmetric Bit Line Sensing Scheme and Quiet Unselected IO Scheme, K.J. Noh, Y.J. Choi, J.D. Joo, M.J. Kim, J.H. Jung, J.J. Lim, C.H. Lee, G.H. Kim, M.G. Kim, Sumsung Electronics Co., Ltd., Gyunggi-do, Korea

A SRAM-like embedded DRAM compiler with 0.13um technology was designed using two novel circuit schemes. Firstly, Dual Asymmetric bit line Sensing Scheme is proposed to implement VDD bit line pre-charge scheme without any reference cells and half charge generator. Therefore, we overcame the risk of failure caused by defects in reference cells and simplified embodying VDD bit line pre-charge scheme, enjoying privileges of VDD bit line pre-charge scheme such as fast sensing speed (tRC:7ns, tAC:6.7ns in this work) and stable sensing operation at low voltage and low temperature. Secondly, we propose circuit idea for quiet unselected IO lines. Unselected IO lines are not developed by bitline data during READ/WRITE operation. This scheme has advantage in the architecture with wide IO and various IO multiplexing options like a memory compiler

Lunch 12:00 pm